AMENDMENTS TO THE DRAWINGS:

The attached drawing(s) include changes to FIGS. 1, 2, 3, and 4 to designate same by the legend - -PRIOR ART- -. Further, responsive to the Examiner's objection, FIG. 10 has been corrected by deleting reference numeral 20 and replacing it with - -200- -.

Replacement Drawings of FIGS. 1-4 and 10 are submitted herewith.

Approval of these changes and entry of the corrected/replacement Drawings is respectfully requested.

REMARKS

In accordance with the foregoing, the specification, Abstract and claims 1-7, 9 and 10 have been amended. No new matter is presented in the foregoing amended specification paragraphs and claims 1-7, 9 and 10 and, accordingly, approval and entry of same are respectfully requested.

STATUS OF CLAIMS

Claims 1-10 are pending and under consideration.

Claims 1-5 are allowed.

Claims 6-10 are rejected.

ITEMS 2 AND 3: OBJECTION TO SPECIFICATION

In response to Item 2, a substitute Abstract is presented in the foregoing.

Responsive to Item 3, Applicant has amended the specification to correct the typographical error notated in Item 3.

ITEMS 4 AND 5: OBJECTIONS TO THE DRAWINGS

In accordance with the foregoing, replacement drawings of FIGS. 1-4 responsive to Item 4 and a replacement drawing of FIG. 10 responsive to Item 5 are herewith submitted.

ITEM 7: REJECTION OF CLAIMS 6-10 FOR OBVIOUSNESS UNDER 35 U.S.C. §102(b) IN VIEW OF NIX (U.S. PATENT 4,897,810)

The rejections are respectfully traversed.

According to Nix, level-triggering type latches (the elements 26/28 and 76/78) are used, in each of which an output level is updated when a reference signal has a predetermined level.

In contrast thereto, according to the present invention, edge-triggering type flip-flops (21, 22 and 23) are used, in each of which an output level is updated when a reference signal has a predetermined edge.

When the level-triggering type latch is employed as in the art of Nix, the following problem may occur:

First, erroneous operation may occur. That is, there may be a possibility that inputs to the OR device 82 (see FIG. 1 of Nix) may have reverse timings, i.e., the lower input (the feed back signal via the NOT device 22) rises up, prior to the rising up of the upper input (directly

from the READ terminal), due to an actual circuit layout, even though the upper input should rise up first only according to the diagrammatic circuit configuration of FIG. 1. If such a phenomenon occurs, an unexpected pulse-like output occurs from the OR device 82, which clears the latch 26/28, and a predetermined data holding period of the output of the flip-flop circuit subsequent to the latch 26/28 cannot be ensured. Thus, Nix's circuit depends from the 'actual circuit layout'.

Thus, a circuit configuration employing such a level-triggering latch depends from an actual circuit layout, and predictably, is not suitable for use in up-to-date LSI technology (FPGA or such) as employed in the present invention.

The present invention is directed to solving this problem. The present invention is implemented consistent with a currently proposed synchronization circuit theory. As a result, a circuit is not likely to depend from an actual circuit layout as is Nix, and thus CAD, such as a static analyzer, may be easily introduced for designing LSI. Further, since the level-triggering latch of Nix, which is not suitable to an LSI circuit, is not employed, a circuit according to the present invention may be applied to any type of LSI.

Accordingly, it is submitted that Nix is clearly not relevant to the present invention, as claimed, and is indisputably incapable of supporting rejections on grounds of anticipation (§102) as raised herein, and as well does not suffice to render the pending claims unpatentable on grounds of obviousness (§103), as would be apparent to one of ordinary skill in the art.

CONCLUSION

It is respectfully submitted that the foregoing demonstrates that the rejected claims 6-10 clearly, patentably distinguish over the art and rejections of record and, along with allowed claims 1-5, are in condition for allowance. There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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Date: March 23, 2006

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